

FIG. 1 is a block diagram of a channel controller system.

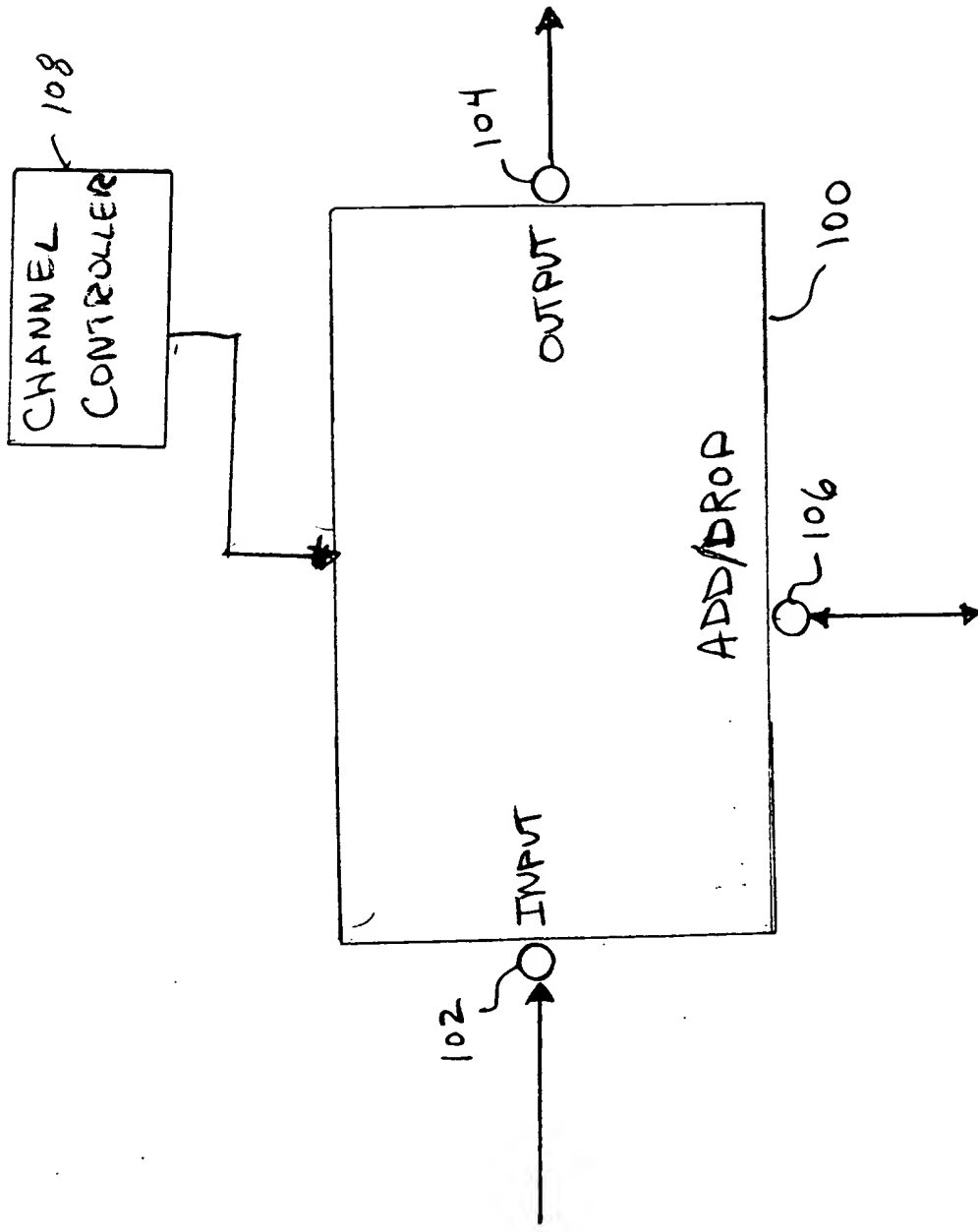
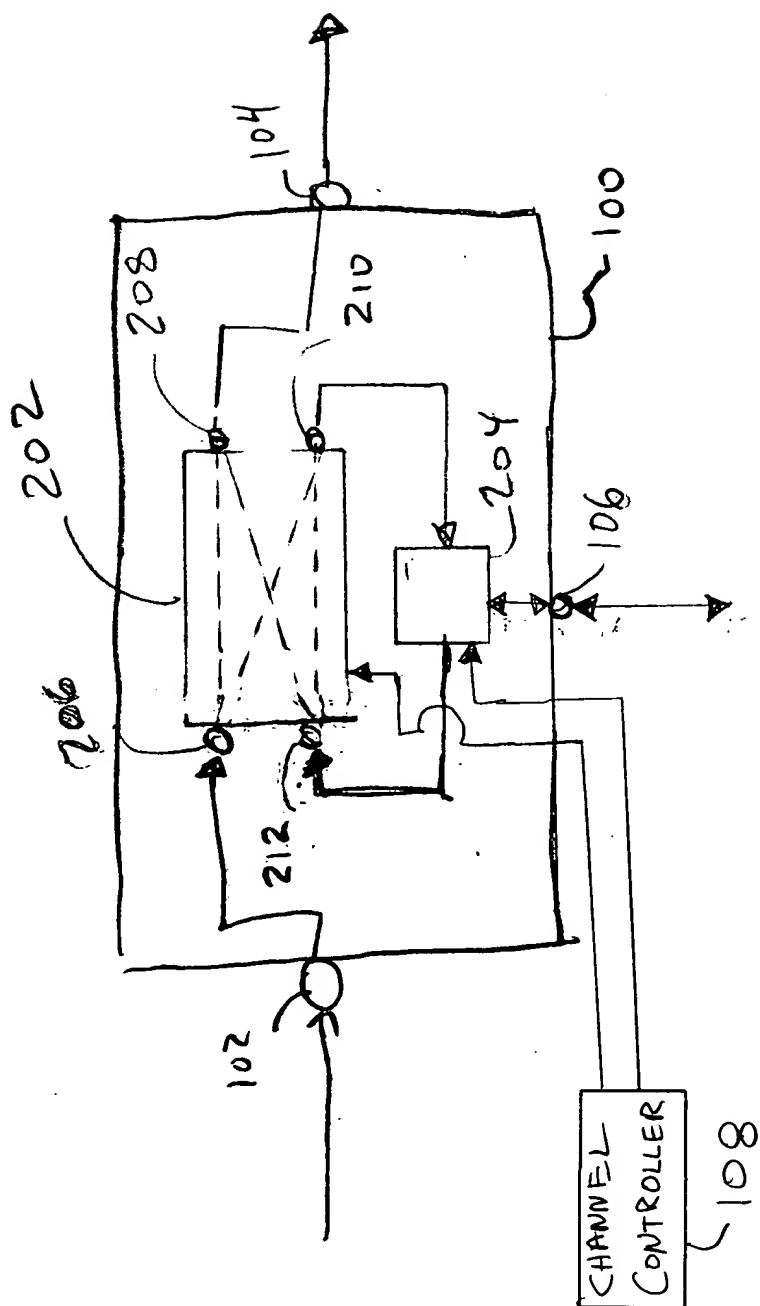


FIG. 1

$\{ \mathbf{e}_1^{(m)}, \mathbf{e}_2^{(m)}, \dots, \mathbf{e}_m^{(m)} \}$ and $\{ \mathbf{e}_1^{(n)}, \mathbf{e}_2^{(n)}, \dots, \mathbf{e}_n^{(n)} \}$ are orthonormal bases for \mathbb{R}^m and \mathbb{R}^n , respectively. Then $\mathbf{e}_i^{(m)}$ and $\mathbf{e}_j^{(n)}$ are orthogonal to each other for all i, j .



2541

FIG. 3 is a schematic diagram of a channel controller system.

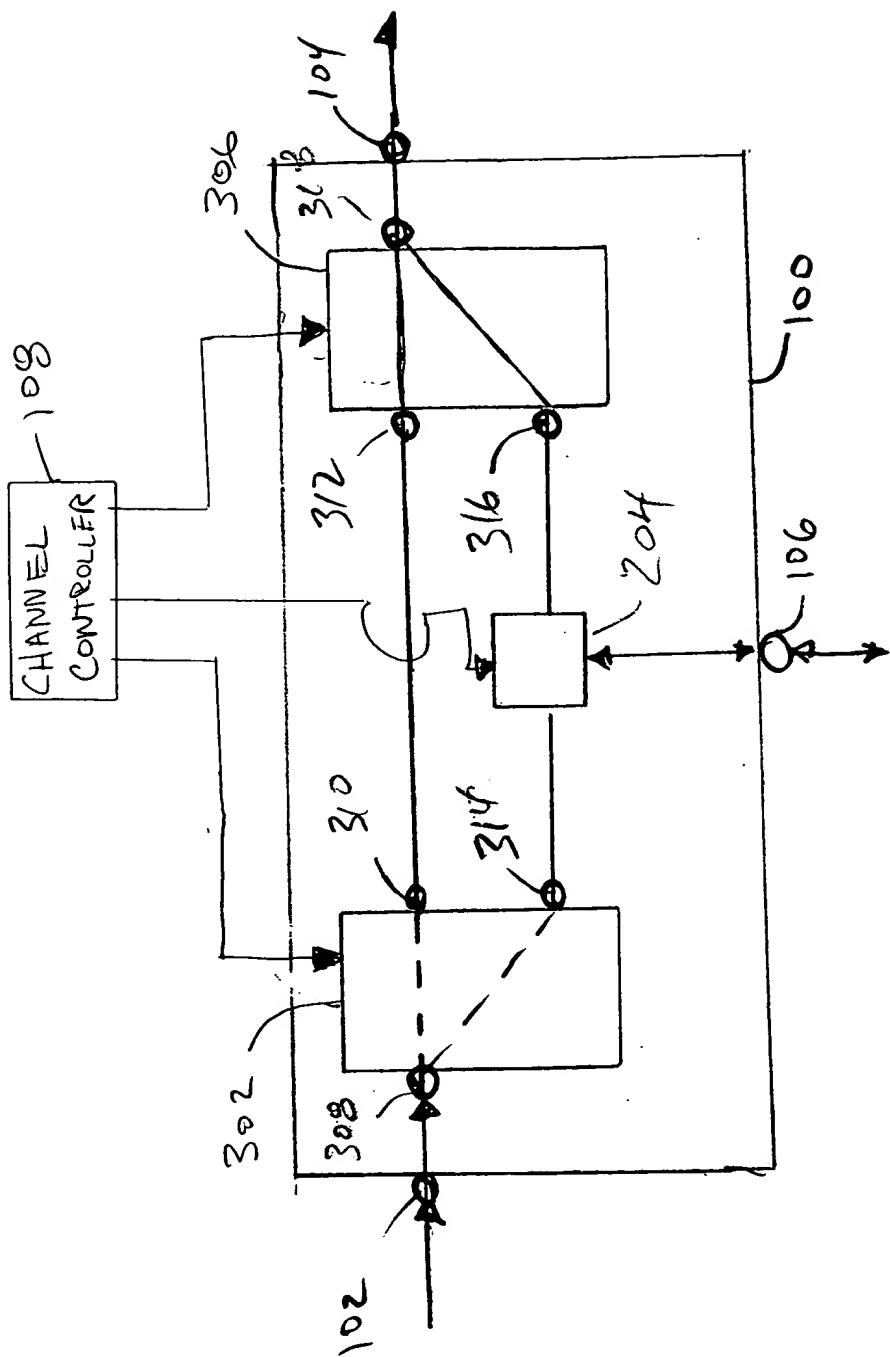
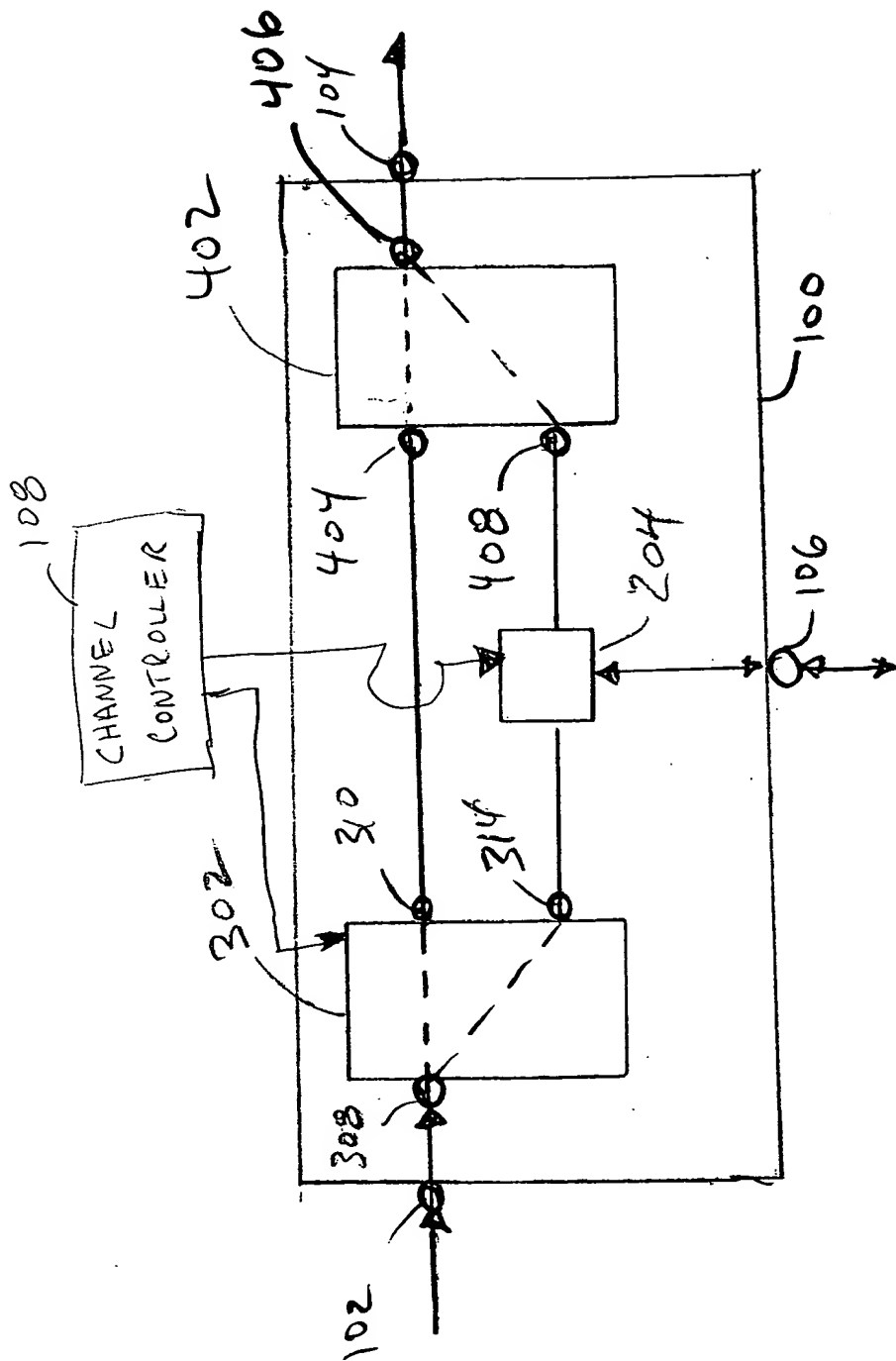


FIG 3



Handwritten signature: H. G. H.

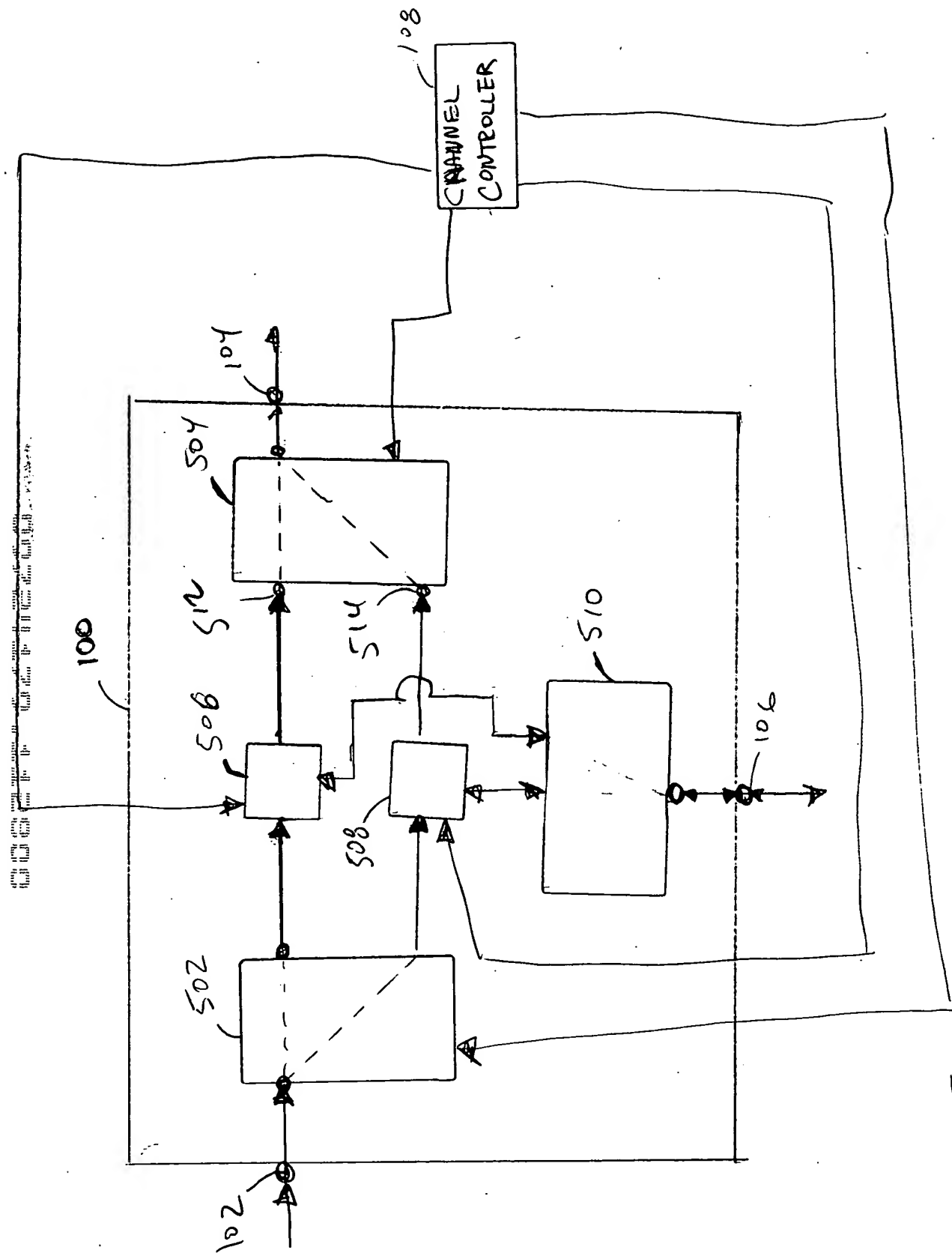


FIG 5

FIG. 6A is a block diagram of a system 100 for controlling a channel controller 108. The system 100 includes a plurality of input devices 602, 604, 606, 608, 610, 612, 614, 616, 618, 620, 622, 624, 626, 628, 630, 632, 634, 636, 638, 640, 642, 644, 646, 648, 650, 652, 654, 656, 658, 660, 662, 664, 666, 668, 670, 672, 674, 676, 678, 680, 682, 684, 686, 688, 690, 692, 694, 696, 698, 700, 702, 704, 706, 708, 710, 712, 714, 716, 718, 720, 722, 724, 726, 728, 730, 732, 734, 736, 738, 740, 742, 744, 746, 748, 750, 752, 754, 756, 758, 760, 762, 764, 766, 768, 770, 772, 774, 776, 778, 780, 782, 784, 786, 788, 790, 792, 794, 796, 798, 800, 802, 804, 806, 808, 810, 812, 814, 816, 818, 820, 822, 824, 826, 828, 830, 832, 834, 836, 838, 840, 842, 844, 846, 848, 850, 852, 854, 856, 858, 860, 862, 864, 866, 868, 870, 872, 874, 876, 878, 880, 882, 884, 886, 888, 890, 892, 894, 896, 898, 900, 902, 904, 906, 908, 910, 912, 914, 916, 918, 920, 922, 924, 926, 928, 930, 932, 934, 936, 938, 940, 942, 944, 946, 948, 950, 952, 954, 956, 958, 960, 962, 964, 966, 968, 970, 972, 974, 976, 978, 980, 982, 984, 986, 988, 990, 992, 994, 996, 998, 1000.

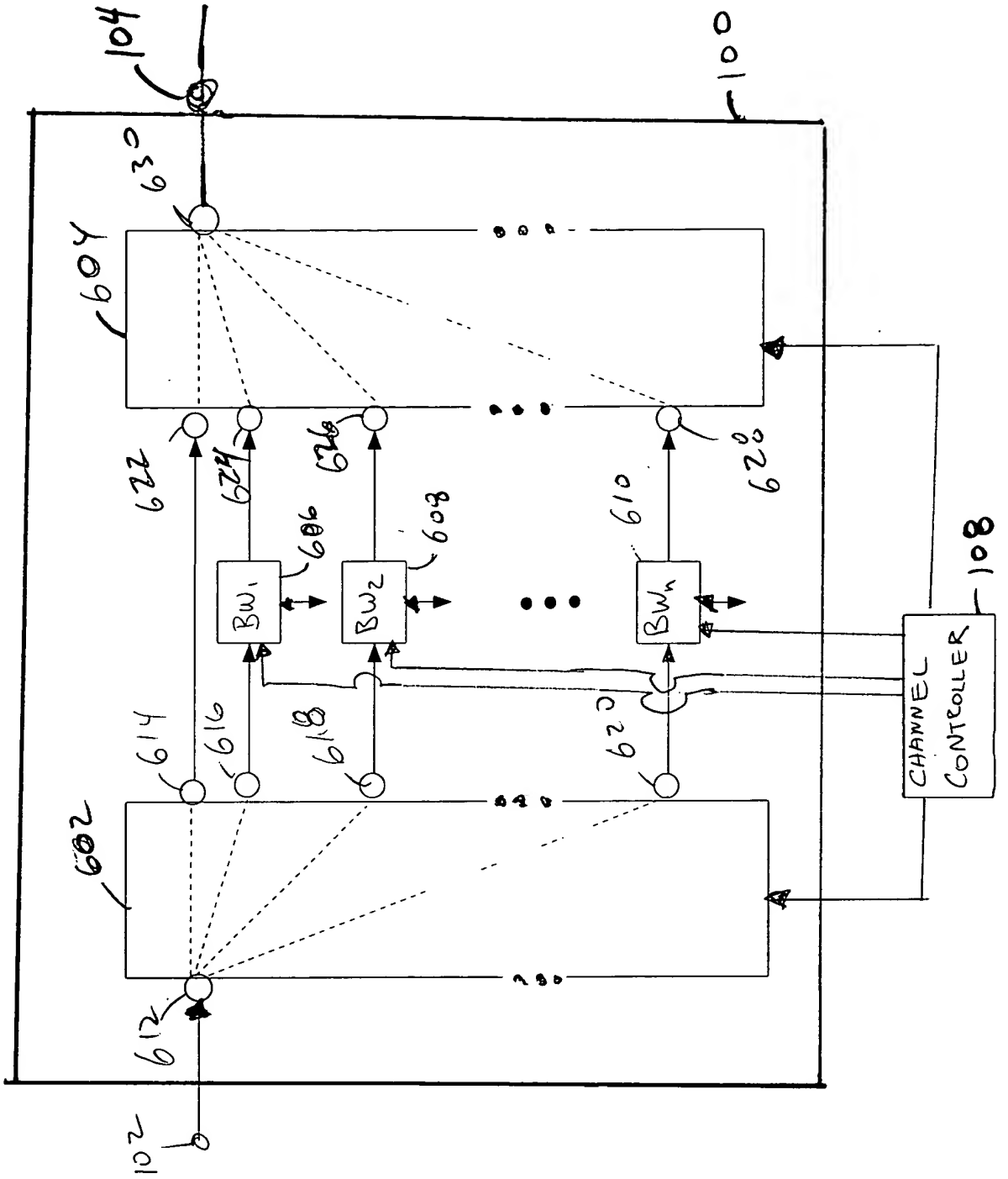


FIG. 6A

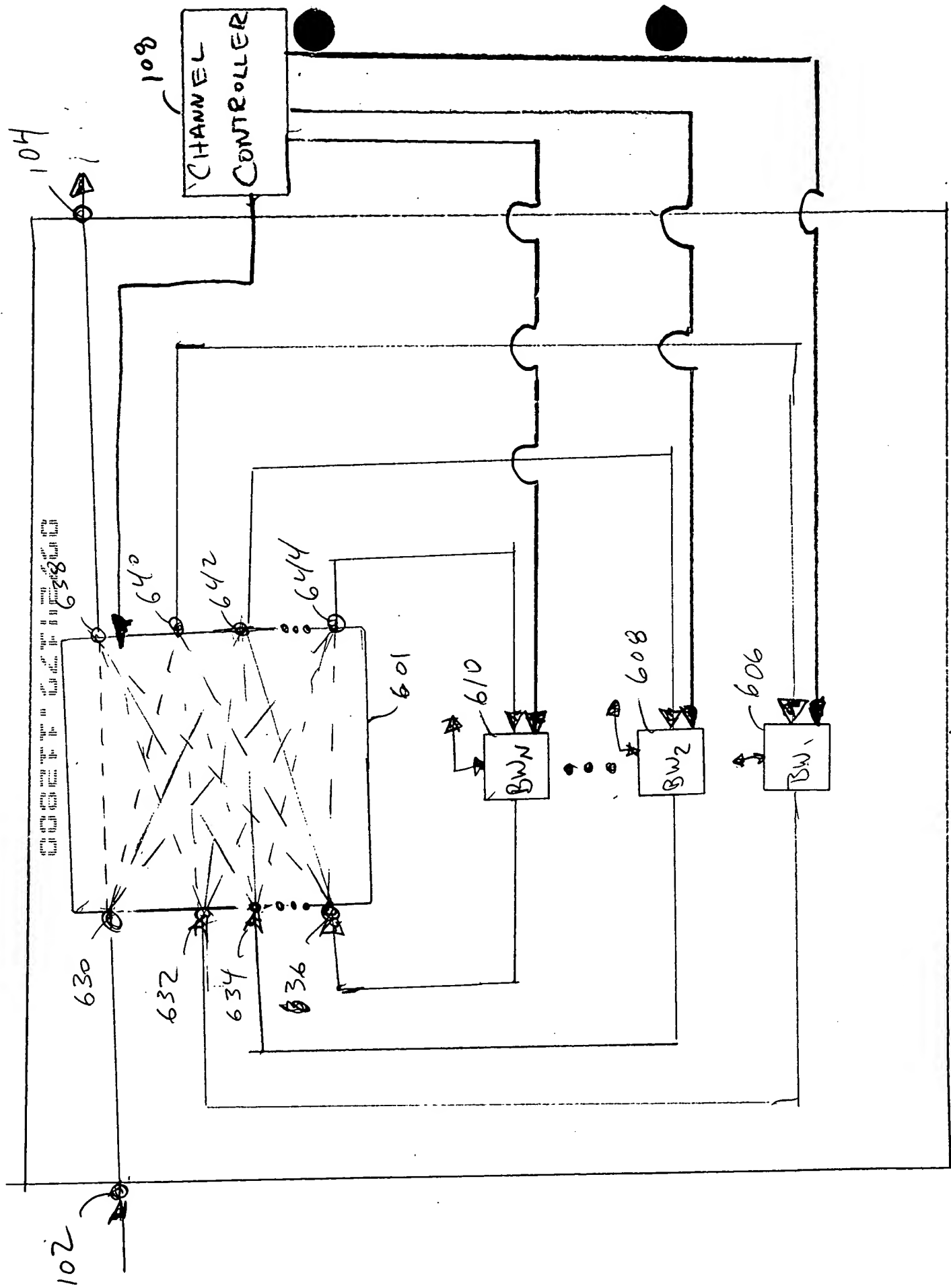


FIG. 6B

100

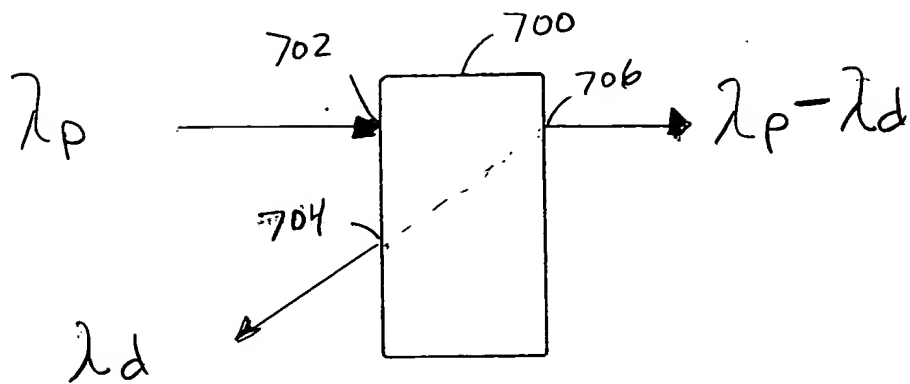


FIG. 7

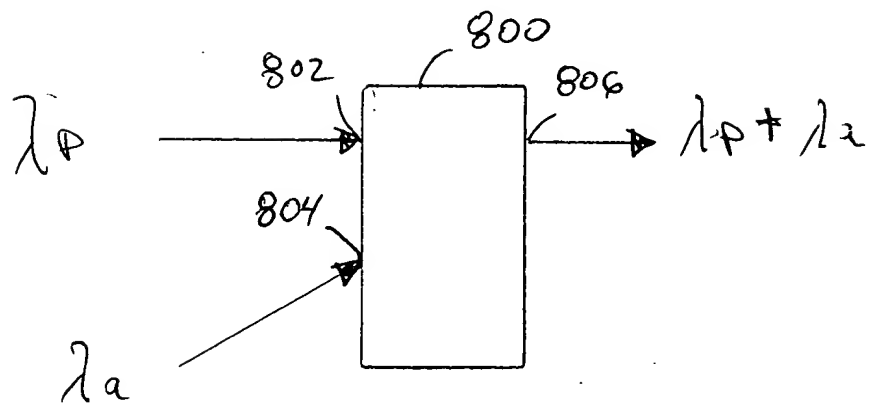


FIG. 8

FIG. 9 is a block diagram of a system for processing a sequence of signals. The system includes three blocks, each labeled 700. The first block receives an input λ_p and produces an output λ_1 . The second block receives an input $\lambda_p - \lambda_1$ and produces an output λ_2 . The third block receives an input $\lambda_p - \lambda_1 - \lambda_2$ and produces an output λ_n . The outputs $\lambda_1, \lambda_2, \dots, \lambda_n$ are summed to produce the final output $\lambda_p - \sum_{k=0}^n \lambda_k$.

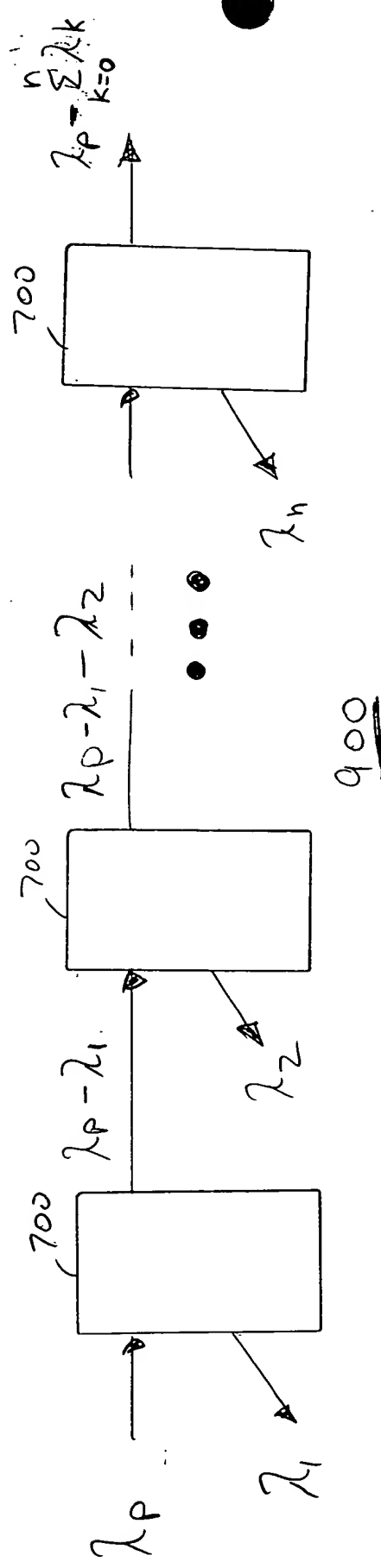


FIG. 9

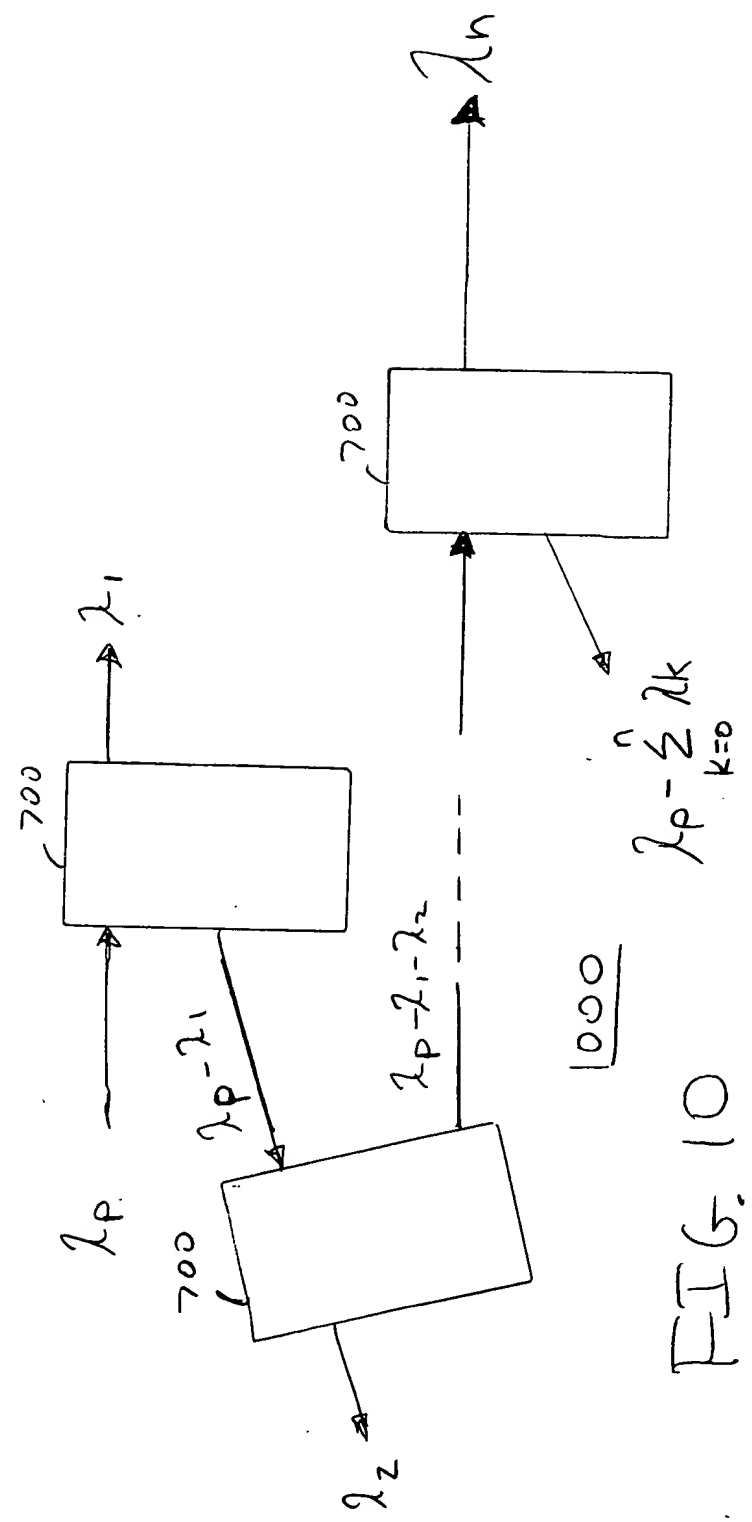
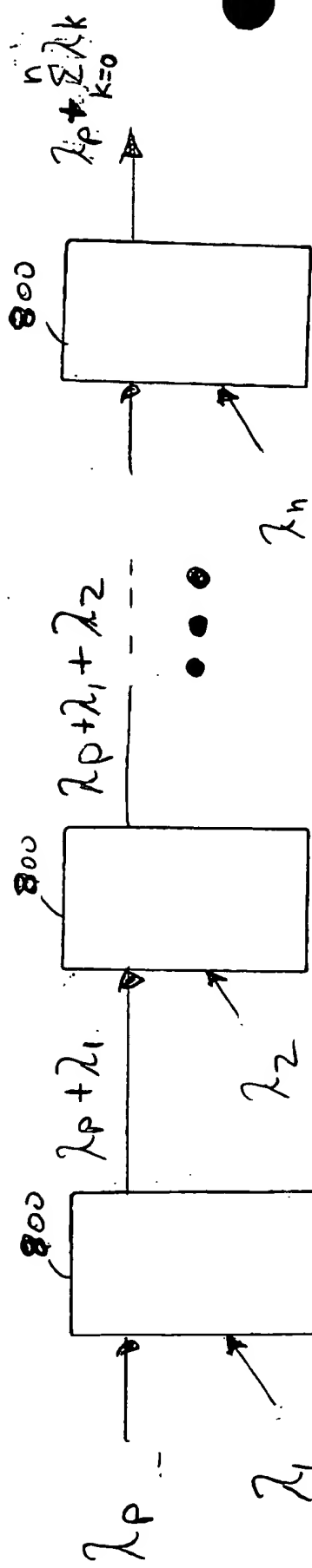


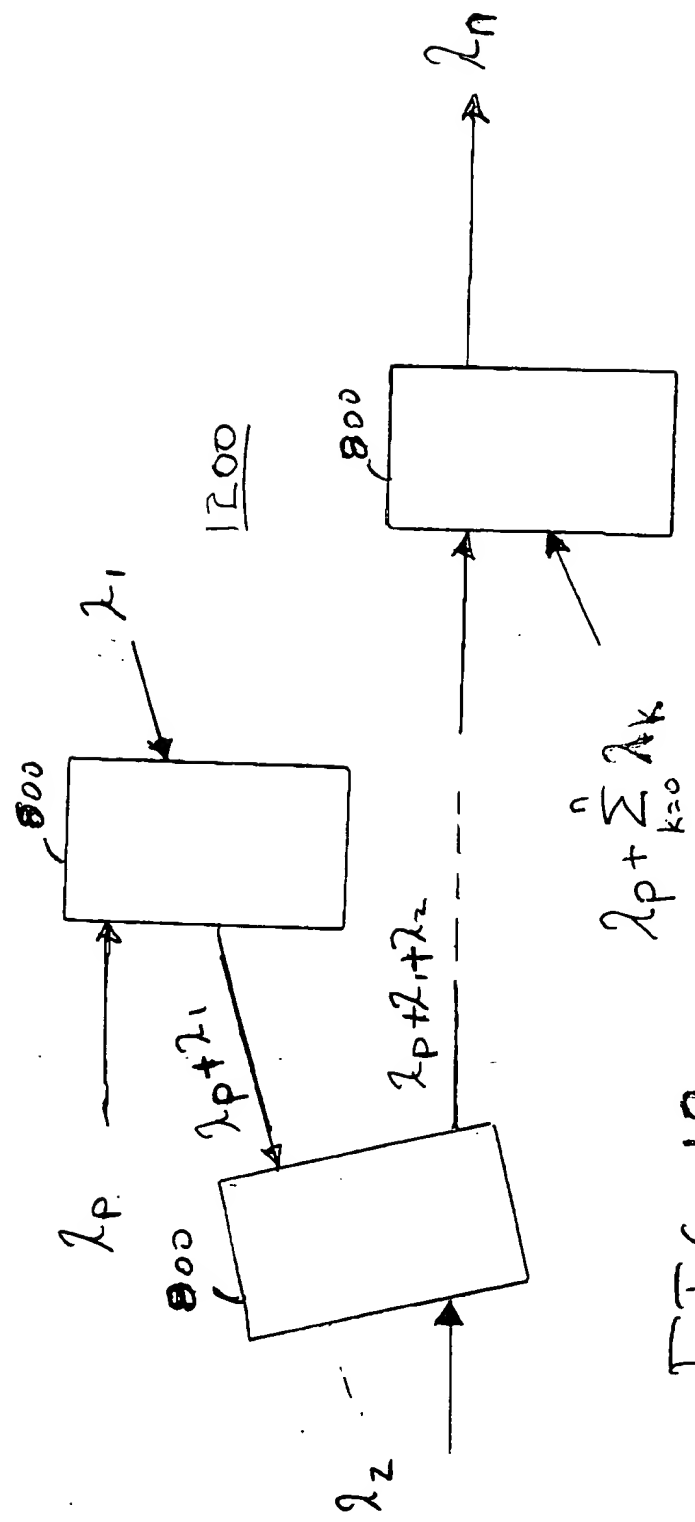
FIG. 10

FIG. 11 is a block diagram of a system for processing a sequence of inputs $\lambda_1, \lambda_2, \dots, \lambda_n$ to produce a final output $\lambda_p + \sum_{k=0}^n \lambda_k$. The system consists of three main processing blocks, each labeled 800, connected in series. The first block takes λ_p and λ_1 as inputs and outputs $\lambda_p + \lambda_1$. The second block takes $\lambda_p + \lambda_1$ and λ_2 as inputs and outputs $\lambda_p + \lambda_1 + \lambda_2$. The third block takes $\lambda_p + \lambda_1 + \lambda_2$ and λ_n as inputs and outputs the final result $\lambda_p + \sum_{k=0}^n \lambda_k$. Ellipses between the second and third blocks indicate that intermediate inputs $\lambda_3, \dots, \lambda_{n-1}$ are processed in a similar manner.



1100

FIG. 11



1200

FIG. 12

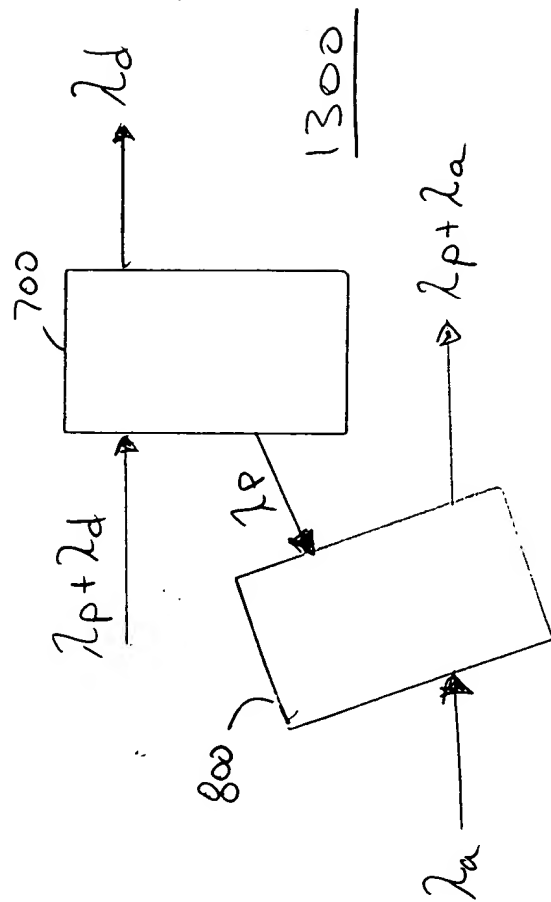


FIG. 13

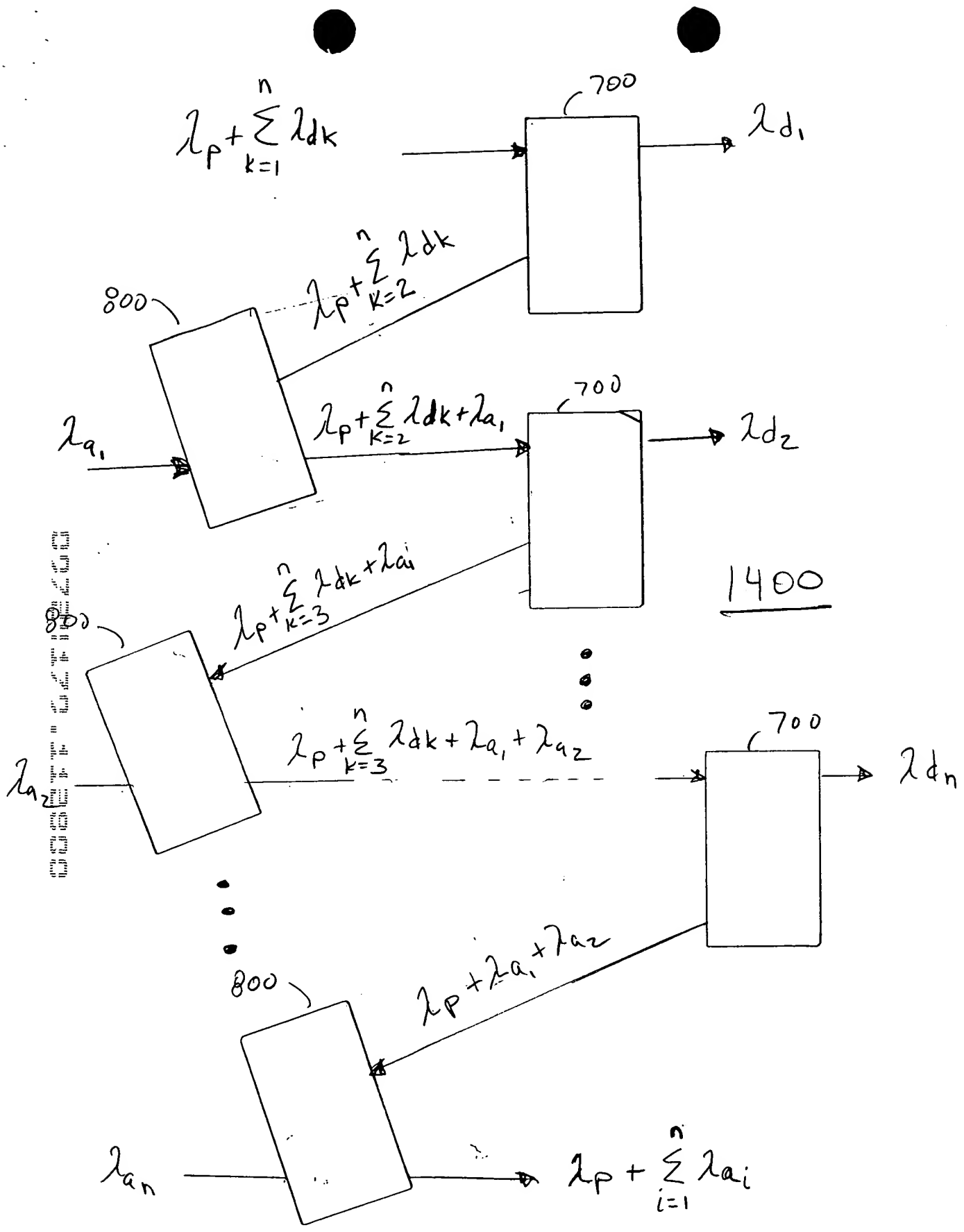


FIG. 14

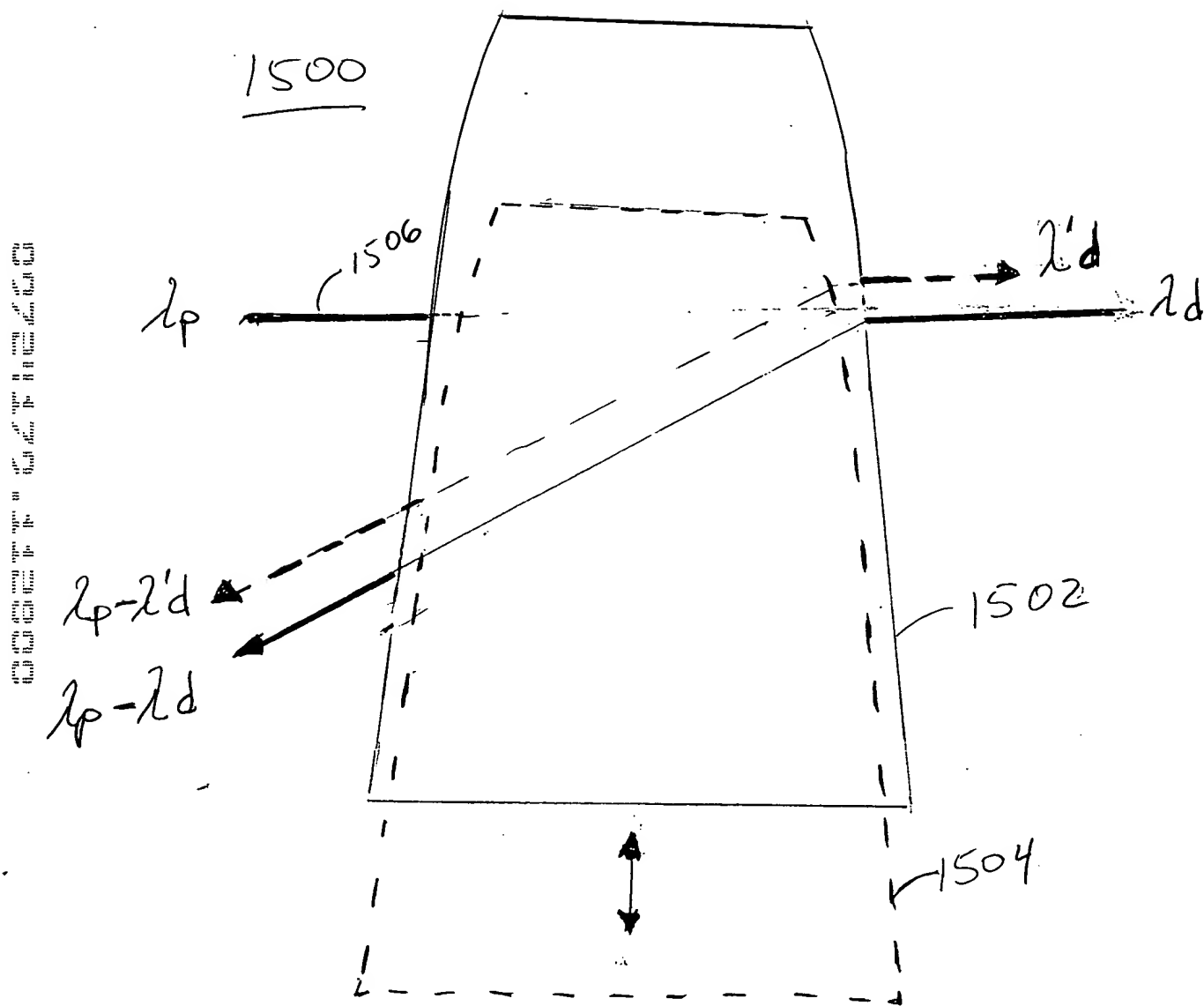


FIG. 15

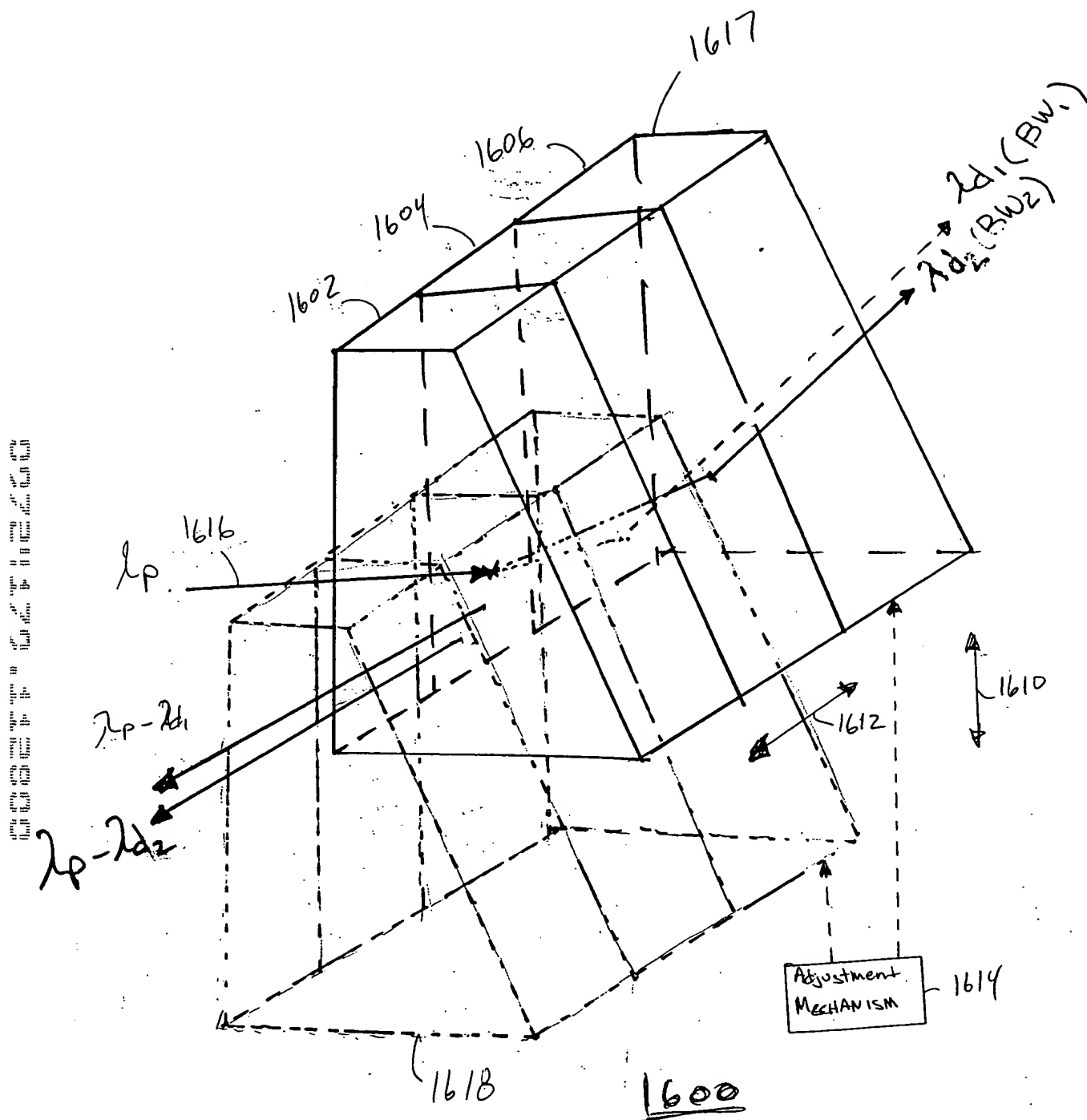
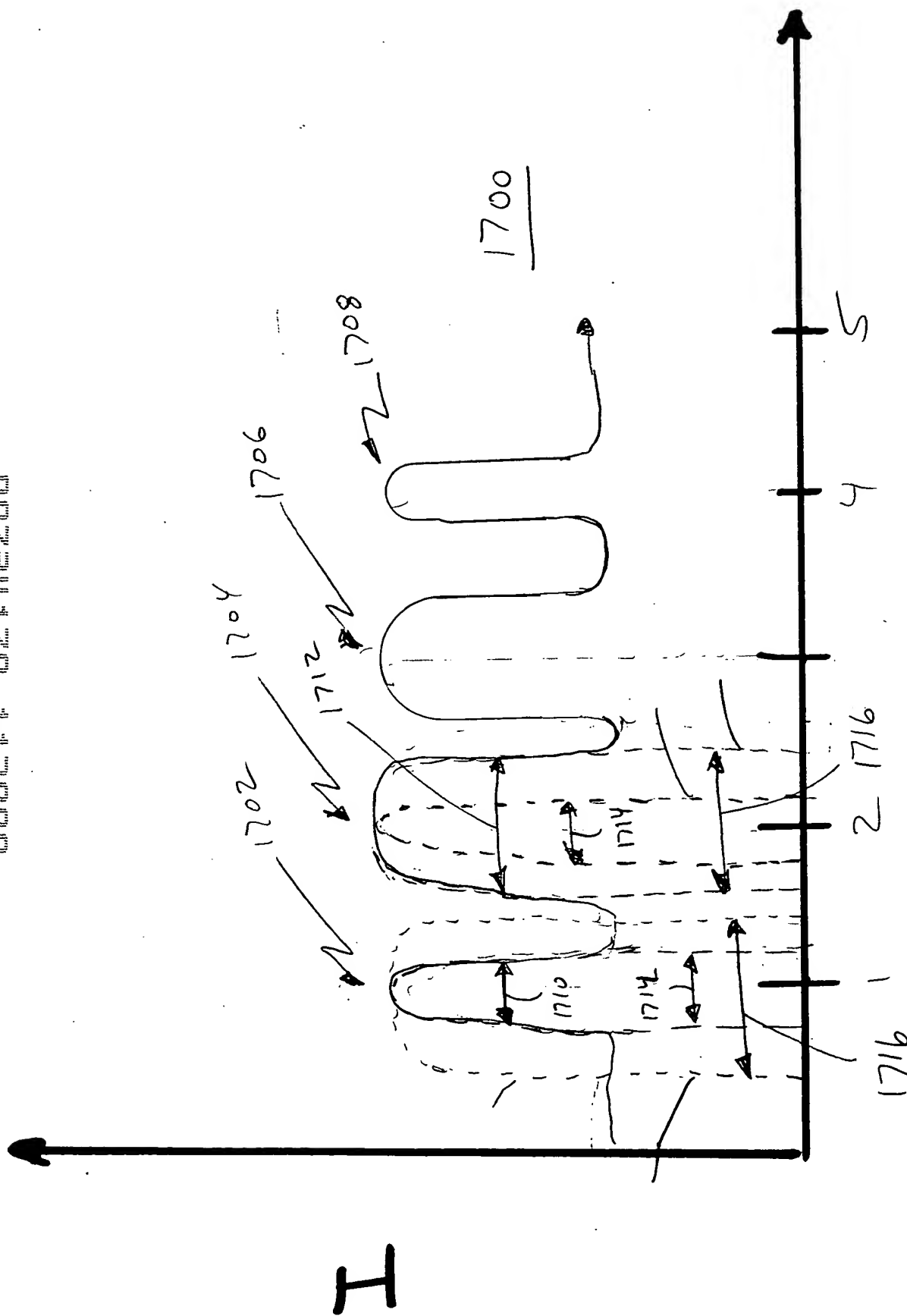


FIG. 16

FIG. 17 is a schematic diagram of a device in accordance with the present invention.



1/2

FIG. 17

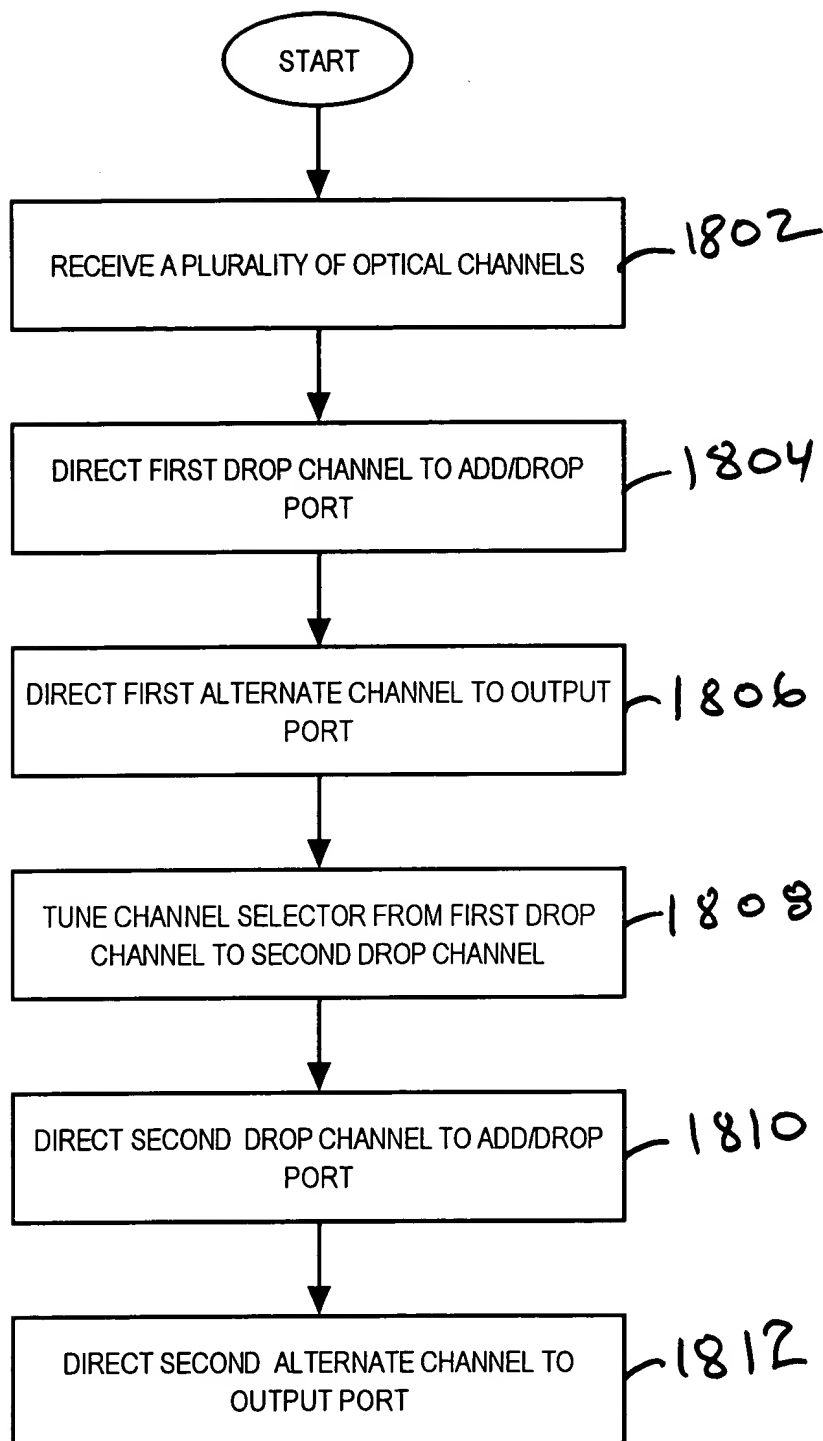


FIG. 18

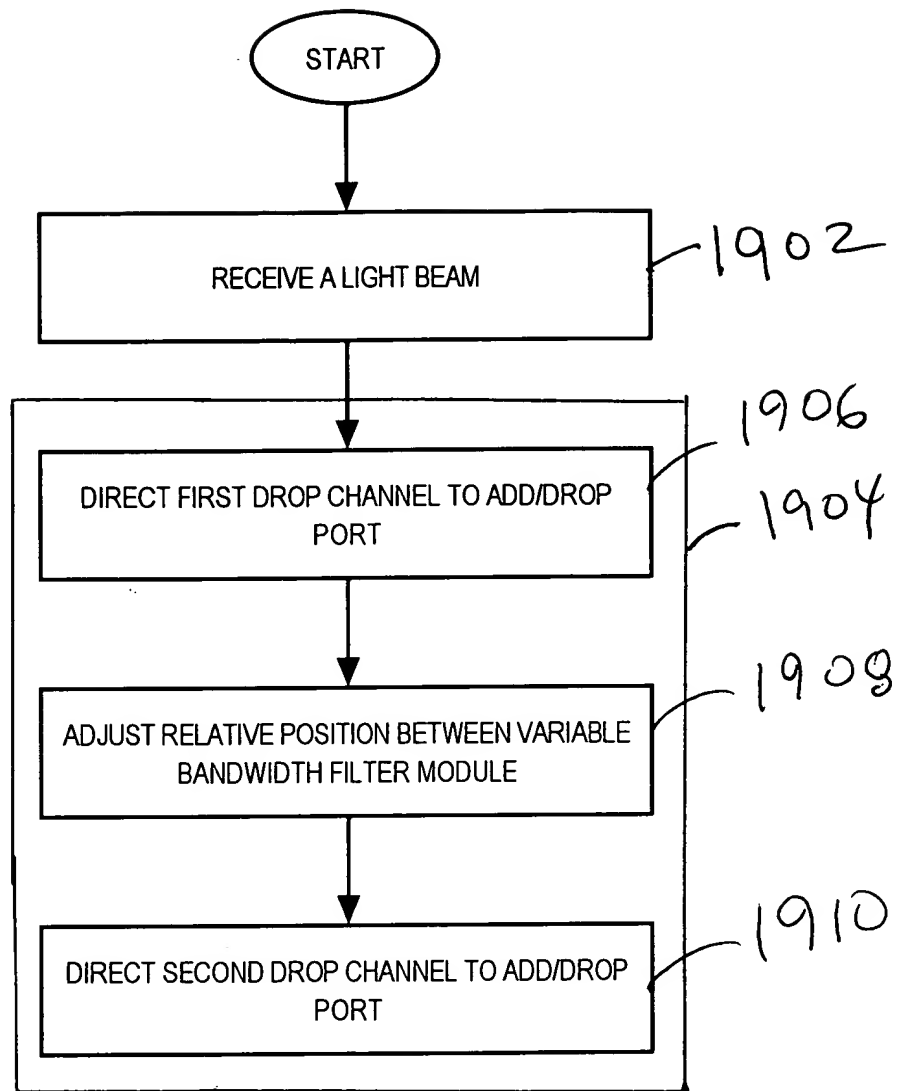


FIG. 19